

Page 14, line 5, replace "FIGs. 15A, 15B and 15C" with --  
FIGs. 15A, 15B, 15C and 15D--.

Page 14, line 17, replace "FIG. 18 is" with --FIGs. 18A and  
18B, arranged as shown in FIG. 18, are--.

Page 15, line 12, replace "FIGs. 24A and 24B" with --FIGs.  
24A, 24B and 24C--.

Page 109, lines 1-2, delete the title of the abstract and  
substitute therefore Memory Controller for Controlling  
Memory Accesses Across Networks in Distributed Shared Memory  
Processing Systems--.

IN THE CLAIMS

Cancel claims 2-30.

Amend claim 1, as follows:

1. [Amended] A cache coherency system for a shared memory parallel processing system including a plurality of processing nodes, comprising: a multi-stage communication network for interconnecting said processing nodes; each said processing node including one or more caches for storing a plurality of cache lines; and a cache coherency directory which is distributed to each of said nodes for tracking which of said nodes have copies of each cache line.

Add new claims 31-39, as follows:

31. A method for operating a shared memory parallel processing system as a cache coherency system including a plurality of processing nodes, comprising the steps of:

interconnecting said processing nodes through a multi-stage communication network;

storing at each said processing node a plurality of cache lines in one or more caches;

distributing to each of said processing nodes a cache

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coherency directory; and

tracking in said cache coherency directory which of  
said processing nodes have copies of each cache line.

32. A program storage device readable by a machine,  
tangibly embodying a program of instructions executable by a  
machine to perform method steps for operating a shared  
memory parallel processing system including a plurality of  
processing nodes, said method steps comprising:

interconnecting said processing nodes through a multi-  
stage communication network;

storing at each said processing node a plurality of  
cache lines in one or more caches; and

tracking in a cache coherency directory which is  
distributed to each of said processing nodes which of  
said processing nodes have copies of each cache line.

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33. An article of manufacture comprising:

a computer useable medium having computer readable program code means embodied therein for operating a shared memory parallel processing system including a plurality of processing nodes, the computer readable program means in said article of manufacture comprising:

computer readable program code means for causing a computer to effect interconnecting said processing nodes through a multi-stage communication network;

computer readable program code means for causing a computer to effect storing at each said processing node a plurality of cache lines in one or more caches; and

computer readable program code means for causing a computer to effect tracking in a cache coherency directory which is distributed to each of said processing nodes which of said processing nodes have copies of each cache line.

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1 34. A computer program product or computer program element  
2 for operating a shared memory parallel processing system  
3 including a plurality of processing nodes according to the  
4 steps of:

5 interconnecting said processing nodes through a multi-  
6 stage communication network;

7 storing at each said processing node a plurality of  
8 cache lines in one or more caches;

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9 distributing to each of said processing nodes a cache  
10 coherency directory; and

11 tracking in said cache coherency directory which of  
12 said processing nodes have copies of each cache line.

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1 35. The cache coherency system of claim 1, further  
2 comprising:

3 a shared memory including a first memory portion for  
4 storing unchangeable data and a second memory portion  
5 for storing changeable data; and

6 said cache coherency directory listing which nodes of  
7 said plurality of processing nodes have accessed copies  
8 of said cache lines in said second memory portion.

1 36. The cache coherency system of claim 35, each of said  
2 plurality of processing nodes being operable for reading,  
3 storing, and invalidating said shared memory at any other of  
4 said processing nodes.

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37. The cache coherency system of claim 36, further  
2 comprising at a first node of said plurality of processing  
3 nodes a memory controller selectively operable first  
4 responsive to a request for access to a memory word for  
5 first accessing the cache at said first node and selectively  
6 operable second responsive to being unable to access said  
7 memory word in said cache at said first node for accessing  
8 said memory word selectively from a cache line in said  
9 memory or from a remote memory and storing said cache line  
10 to said cache at said first node.